CLAIMS

What is claimed is:

1. A component comprising:

a clock generator to switch from a first clock frequency to a second clock frequency while the component is in a sleep state, the switch from the first to the second clock frequency to be associated with a transition between a high performance state and a low power state; and

a core to receive a voltage to switch from a first voltage level to a second voltage level while the component is in an active mode, the switch from the first voltage level to the second voltage level to be associated with the transition between the high performance state and the low power state.

2. The component of claim 1, wherein the component includes a cache, the contents of the cache to be maintained during the transition between the high performance state and the low power state.

3. The component of claim 1, wherein the component is a graphics controller.

4. The component of claim 1, wherein the component is a processor to execute instructions during the active mode.

5. The component of claim 4, wherein the active mode is a C0 mode.

6. A voltage regulator comprising:

an output to provide a voltage at a first voltage level;

an input to receive a signal to indicate that the voltage is to switch to a second voltage level; and

a component to switch the voltage from the first voltage level to the second voltage level in a stepwise ramp.

7. The voltage regulator of claim 6, further comprising a voltage level table associated with the ramp.

8. The voltage regulator of claim 7, wherein the voltage level table is to ramp the voltage in 25mV - 50mV steps.

9. The voltage regulator of claim 6, wherein the signal is to further indicate the second voltage level.

10. A system comprising:

a component to switch its clock frequency from a first clock frequency to a second clock frequency while the component is in a sleep state, the switch from the first to the second clock frequency to be associated with a transition between a high performance state and a low power state; and

a voltage regulator to switch a core voltage to the component from a first voltage level to a second voltage level while the component is in an active mode, the switch from the first to the second voltage level to be associated with the transition between the high performance state and the low power state.

11. The system of claim 10, wherein the component includes a cache, the contents of the cache to be maintained during the transition between the high performance state and the low power state.

12. The system of claim 10, wherein the component is a graphics controller or a processor.

13. The system of claim 10, further comprising a voltage level table according to which the core voltage is to switch from the first voltage level to the second voltage level in a stepwise ramp.

14. The system of claim 13, wherein the voltage level table is to ramp the core voltage in 25mV – 50mV steps.

15. A method comprising:

switching a clock generator of a component from a first clock frequency to a second clock frequency while the component is in a sleep state, the switch from the first to the second clock frequency associated with a transition between a high performance state and a low power state; and

switching a core voltage from a first voltage level to a second voltage level while the component is in an active mode, the switch from the first voltage level to the second voltage level associated with the transition between the high performance state and the low power state.

16. The method of claim 15, further comprising maintaining contents of the cache during the transition between the high performance state and the low power state.

17. The method of claim 15, wherein the switching of the core voltage is done in accordance with a voltage level table.

18. A machine-readable medium including machine-readable instructions that, if execute by a computer system, cause the computer system to perform a method comprising:

switching a clock generator of a component from a first clock frequency to a second clock frequency while the component is in a sleep state, the switch from the first to the second clock frequency associated with a transition between a high performance state and a low power state; and

switching a core voltage from a first voltage level to a second voltage level while the component is in an active mode, the switch from the first voltage level to the second voltage level associated with the transition between the high performance state and the low power state.

19. The machine-readable medium of claim 18, wherein the method further comprises maintaining contents of the cache during the transition between the high performance state and the low power state.

20. The machine-readable medium of claim 18, wherein the switching of the core voltage is done in accordance with a voltage level table.